



(19)

Generated Document

(11) Publication number: **01268064 A****PATENT ABSTRACTS OF JAPAN**(21) Application number: **63095564**(51) Int. Cl.: **H01L 29/78 H01L 21/205 H01L 27/10**(22) Application date: **20.04.88**

(30) Priority:

(43) Date of application publication: **25.10.89**

(84) Designated contracting states:

(71) Applicant: **HITACHI LTD**(72) Inventor: **HASHIMOTO KOJI
KAWAMOTO YOSHIFUMI
KOBAYASHI TAKASHI**

(74) Representative:

**(54) FORMATION OF
POLYCRYSTALLINE
SILICON THIN FILM**

(57) Abstract:

PURPOSE: To make it possible to manufacture a polycrystalline Si MOS type field-effect transistor characterized by a small OFF current, a small absolute value of threshold voltage and a large operating current, by using disilane or trisilane as a reacting gas, performing deposition in an amorphous state at a specified temperature, performing a heat

treatment and polycrystallization.

CONSTITUTION: Decomposition is performed at a temperature of 550°C or less by using disilane or trisilane as a reacting gas, and deposition is performed under an amorphous state. Heat treatment is performed at a temperature higher than the deposition temperature, and a polycrystalline state is obtained. For example, an amorphous Si film 13 is deposited on an SiO₂ film 12 on a P-type Si substrate 11 by an LPCVD method by using Si₂H₆ gas as a reacting gas at a temperature of 520°C. The film is patterned in an island shape. Thereafter, an SiO₂ film 14 is deposited. Heat treatment is performed at 900°C, and a gate oxide film is obtained. Then, P ions are implanted in the polycrystalline Si 13. A polycrystalline Si film is deposited by using SiH₄ as a reacting gas, and a gate electrode 15 is formed. Then, an SiO₂ film is formed by heat treatment. BF₂ ions are implanted, and P-type high concentration impurity regions for a source, a drain and a gate are formed.

COPYRIGHT: (C)1989, JPO&Japio